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(54) Abstract Title
Method for fabricating thin film transistor

(57) A method of fabricating a thin film transistor comprises crystallizing an amorphous silicon layer 22 having sloping surface and flat surface by SLS technique using a laser beam having predetermined energy density so as to melt the sloping surface as well as the flat surface of the amorphous silicon layer 22 to form a crystallized silicon layer 23 and forming the active layer by selectively etching the crystallized silicon layer. The laser beam is applied non-vertically to the sloping surface while the laser beam is applied vertically to the flat surface. Although the sloping surface and the flat surface of the amorphous silicon layer 22 are irradiated with laser beam having same laser energy density, the absorbed energy density of the sloping surface may be lower than that of the flat surface. The laser beam requires first energy density to substantially melt the sloping surface and second energy density to substantially melt the flat surface of the amorphous silicon 22. The amorphous silicon layer 22 is irradiated with the laser beam having the first energy density to substantially melt both the sloping and flat surfaces.

FIG.2B

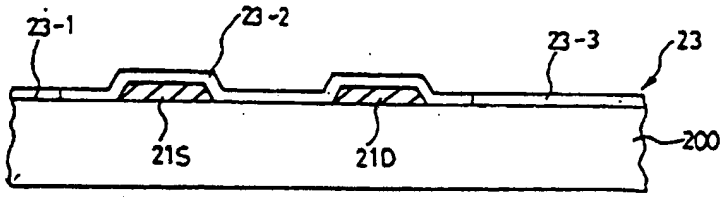

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FIG. 1A (Prior Art)

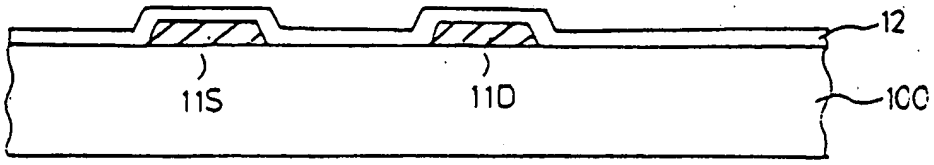


FIG. 1B (Prior Art)

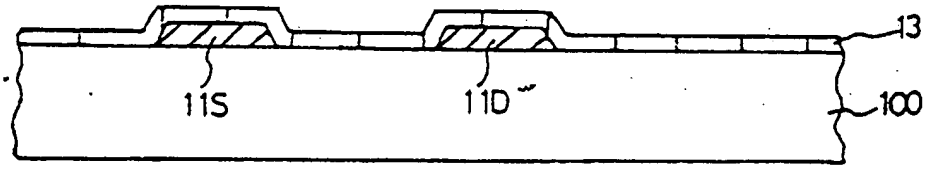


FIG. 1C (Prior Art)

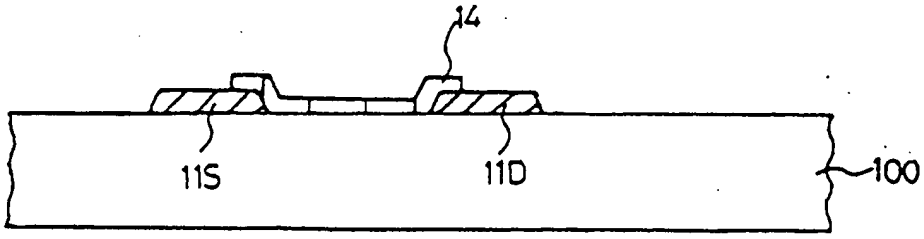


FIG. 1D(Prior Art)

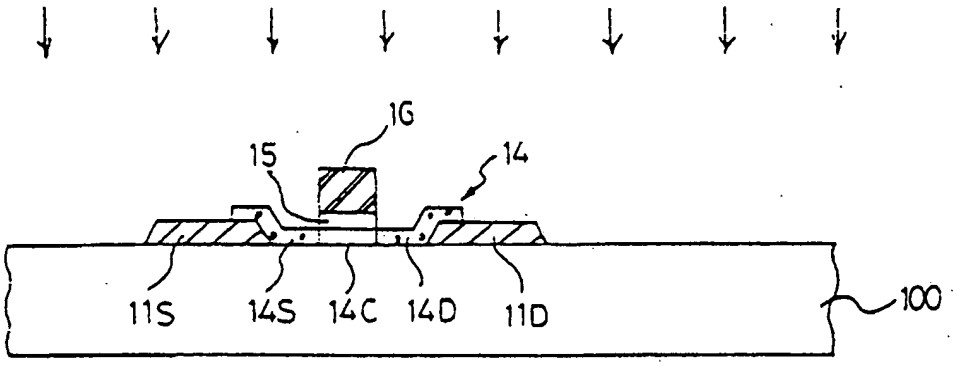


FIG. 1E(Prior Art)

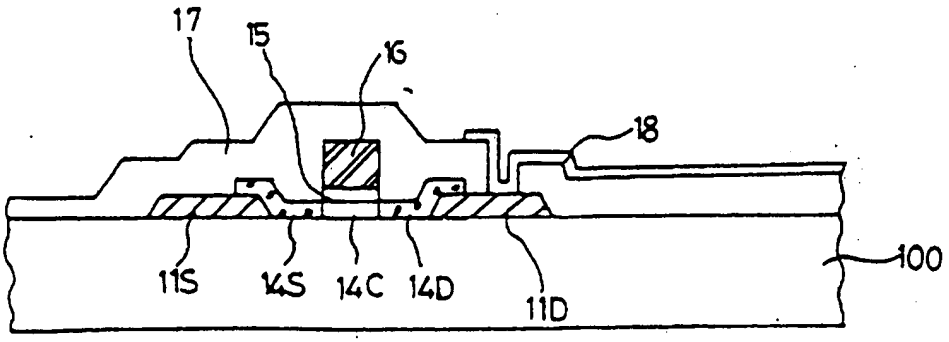


FIG.2A

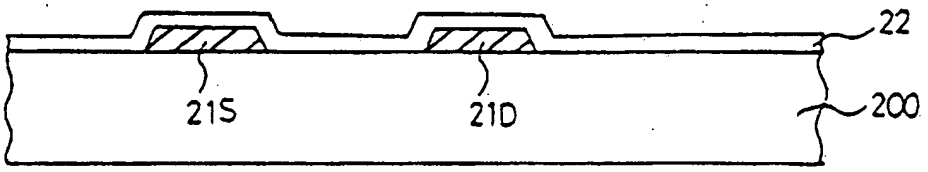


FIG.2B

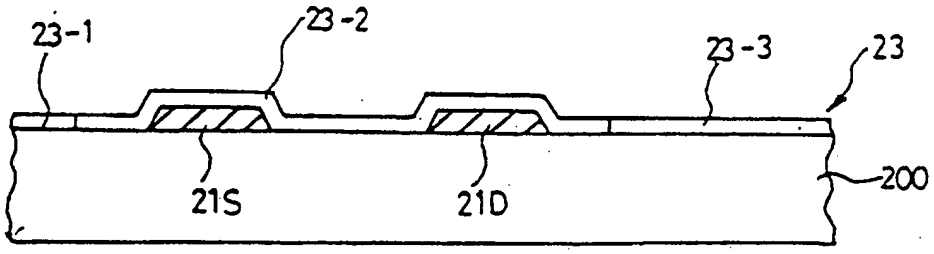


FIG.2C

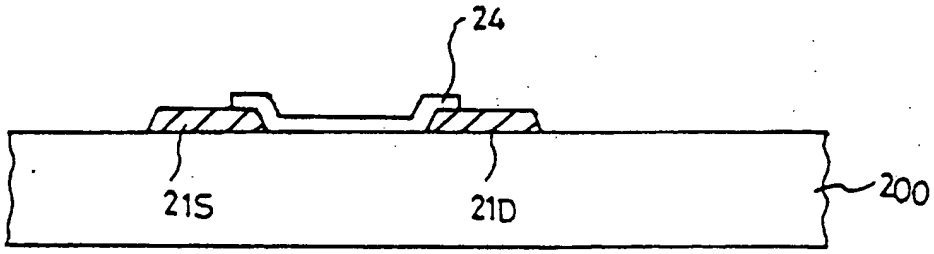


FIG.2D

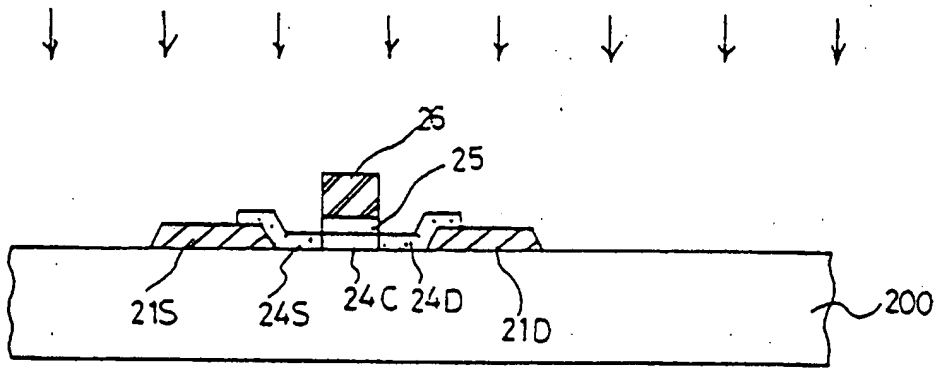


FIG.2E

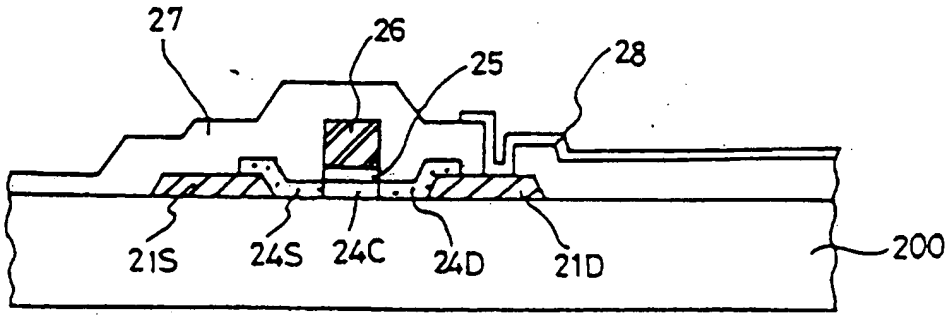


FIG.3

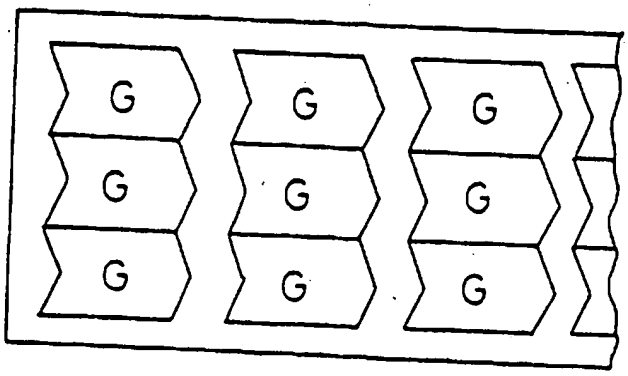


FIG.4

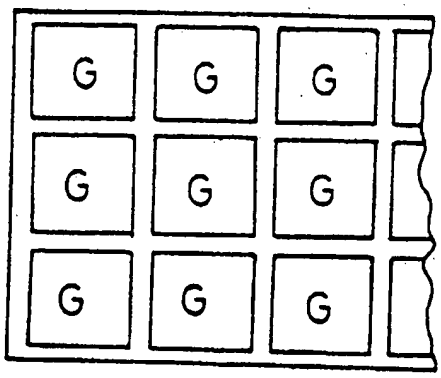


FIG.5

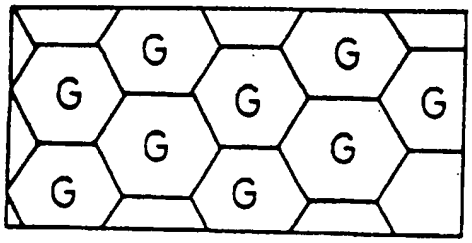


FIG. 6A

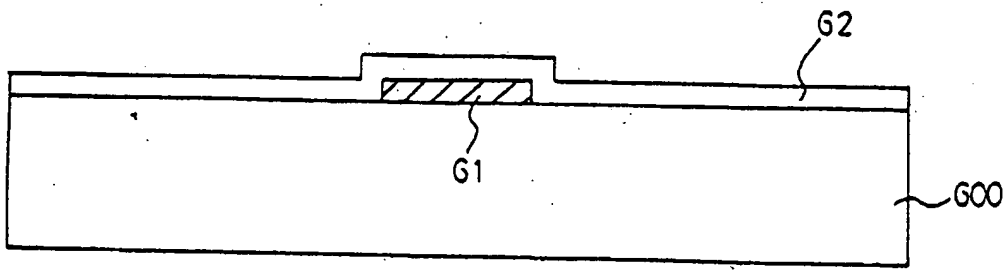


FIG. 6B

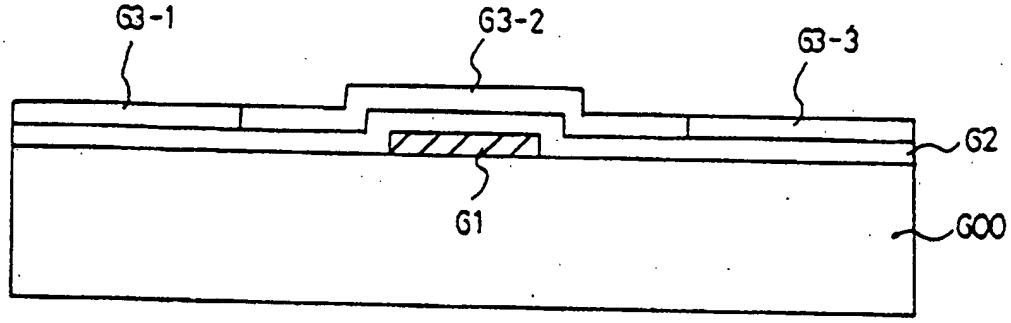


FIG. 6C

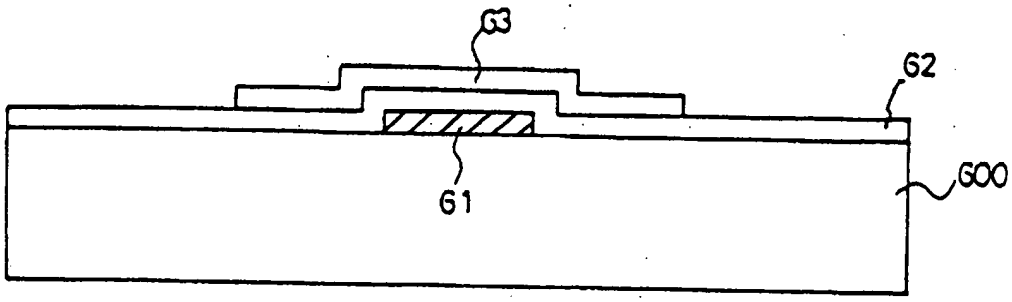


FIG. 6D

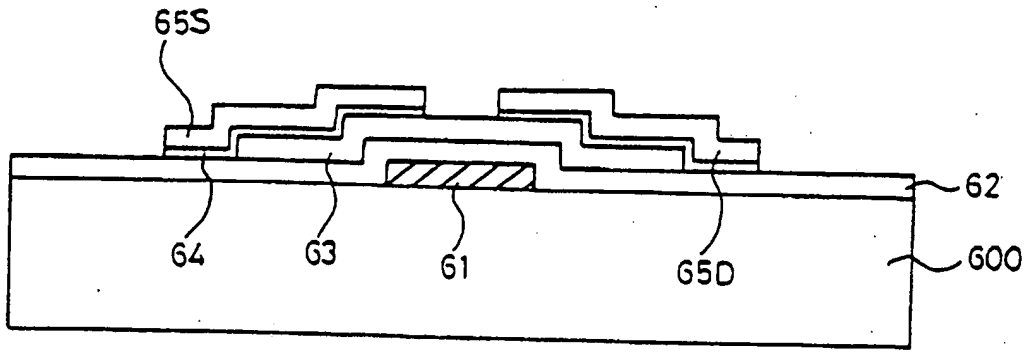
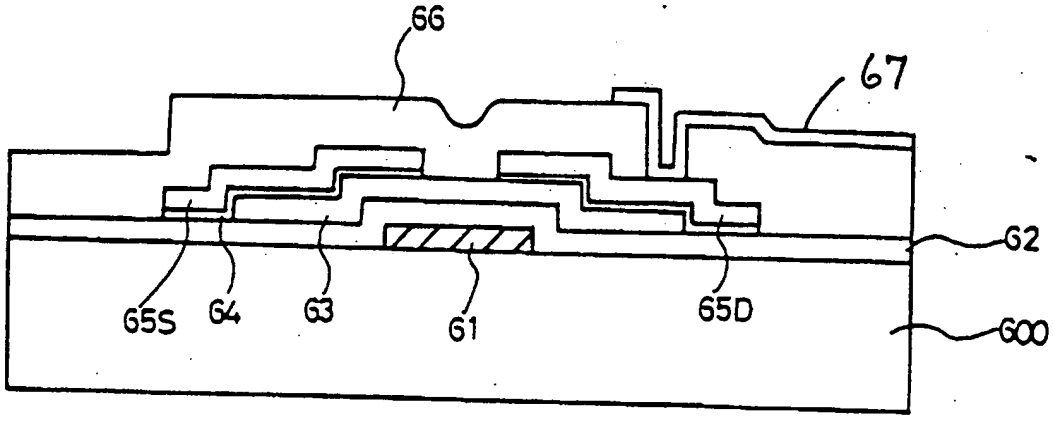


FIG. 6E



METHOD FOR FABRICATING THIN FILM TRANSISTOR

The present invention is related to a method for fabricating Thin Film Transistor (TFT), and more particularly, to a method for fabricating TFT, of which an active layer is formed by crystallizing a silicon thin film, using Sequential Lateral Solidification (SLS).

In order to fabricate TFTs on a low heat-resistant substrate, such as a glass substrate, an amorphous silicon layer or a polycrystalline silicon layer is deposited on the substrate and is etched by photolithography to form active layers for TFTs.

The mobility of a carrier is low in the amorphous silicon layer. Accordingly, amorphous silicon TFT is difficult to be used as a device for driving circuits of a liquid crystal display (LCD). However, the mobility of a carrier is high in the polycrystalline layer. Accordingly, polycrystalline TFT could be used as a device for driving circuits of a liquid crystal display (LCD), in which devices for pixel array and a device for driving circuits are formed simultaneously.

There are two techniques to form polycrystalline silicon film on a glass substrate. The first technique is that an amorphous silicon film is deposited on the substrate and is crystallized under a temperature of 600 by Solid Phase Crystallization (SPC). The first technique needs a high temperature process. Therefore, it is difficult to form the polycrystalline silicon film layer on the glass substrate by the first technique.

The second technique is that an amorphous silicon film is deposited on the substrate and is crystallized by

thermal treatment using a laser. The second technique does not require a high temperature process. Therefore, the second technique is applied to form a polycrystalline silicon film on the glass substrate.

Fig. 1A to Fig. 1E are schematic drawings for explaining a method for fabricating a TFT according to prior art.

Referring to Fig. 1A, a source electrode 11S and a drain electrode 11D are formed on an insulating substrate 100. And an amorphous silicon layer 12 is deposited on the exposed surface of the substrate comprising the source electrode 11S and the drain electrode 11D. Herein the amorphous silicon layer 12 has steps and sloping surfaces, since the amorphous silicon layer 12 covers the protruding source and drain electrodes 11S and 11D.

Referring to Fig. 1B, the amorphous silicon layer is crystallized into a polycrystalline silicon layer 13 by carrying out a crystallization procedure using laser annealing. The method for crystallizing the amorphous silicon layer into the polycrystalline silicon layer 13 by applying a laser beam to the amorphous silicon layer is described as follows.

An active layer of the TFT is formed by the polycrystalline silicon layer having large silicon grains to decrease the effect of the grain boundary which prevents carriers from passing their channel.

A selected region of the amorphous silicon layer is first irradiated at an energy density to induce separated islands of amorphous silicon remaining and the other portions complete melting. The amorphous film is translated relative to the laser beam over a distance less than the predetermined distance for a second

irradiating. While the film is translating, the separated islands of amorphous silicon are used as seeds and grow into the molten silicon region, thereby to form a first polycrystalline silicon region. Herein, grain growth occurs from the interface between the liquid silicon region and the solid state amorphous silicon region into the liquid silicon region. This grain growth stops by making grain boundary when each grain collides. This process, the above-described process of the irradiating and crystallizing, was repeated over a total translation distance to crystallize the majority of the film.

Referring to Fig. 1C, the polycrystalline silicon layer is etched by photolithography to form an active layer 14. Referring to Fig. 1D, a gate insulating interlayer 15 and a gate electrode 16 are formed on the active layer 14. Source and drain regions 14S and 14D are then formed in the active layer 14 by doping impurities in the exposed portions of the active layer 14. The channel region 14C is formed between the source and the drain regions 14S and 14D.

Referring to Fig. 1E, a passivation layer 17 is deposited on the exposed surface of the substrate and is etched selectively to expose a portion of the drain electrode 11D. And a pixel electrode 18 is formed connecting the exposed portion of the drain electrode 11D on the passivation layer 17.

However, since the size of each silicon grain is non-uniform and the location of grain boundary is random in the active layer, device-to-device uniformity is degraded in TFTs fabricated according to the prior art. Therefore, the polycrystalline silicon layer could not be

applied to form devices for complicated circuits, while a single crystal silicon film could be applied to form them.

Accordingly, the present invention is directed to a method for crystallizing an amorphous silicon layer and a method for fabricating a TFT, that substantially obviates one or more of the problems due to limitations and disadvantages of the prior art.

Another object of the present invention is to provide a method for fabricating a TFT, the active layer of which is formed by crystallizing a silicon thin film, using steps by Sequential Lateral Solidification (SLS).

A further object of the present invention is to provide a method for fabricating a TFT, the active layer of which is formed by using a large single silicon grain.

Additional features and advantages of the invention will be set forth in the description which follows and in part will be apparent from the description, or may be learned by practice of the invention. The objectives and other advantages of the invention will be realized and attained by the structure particularly pointed out in the written description and claims hereof as well as the appended drawings.

To achieve these and other advantages and in accordance with the purpose of the present invention, as embodied and broadly described, the present invention, a method for fabricating a TFT having an active layer formed by crystallizing an amorphous silicon layer, comprises forming the active layer having sloping and flat surfaces by selective etching of the crystallized

silicon layer; crystallizing the amorphous silicon layer by SLS technique, using a laser beam having energy density so as to melt the sloping surface as well as the flat surface of the amorphous silicon layer.

In another aspect of the present invention, a method for fabricating a TFT comprises steps of: forming source and drain electrodes on a substrate; depositing an amorphous silicon layer on the exposed portion of the substrate comprising the source and the drain electrodes; crystallizing the amorphous silicon layer by SLS technique; forming an active layer by etching the crystallized silicon layer through photolithography; forming a gate electrode and a gate insulating layer on the active layer; and forming source and drain regions in the active layer by doping impurities selectively in the exposed portion of the active layer.

In another aspect of the present invention, a method for fabricating a TFT, comprising steps of: forming a gate electrode on a substrate; forming a gate insulating layer on the exposed portion of the substrate comprising the gate electrode; depositing an amorphous silicon layer on the exposed portion of the gate insulating layer; crystallizing the amorphous silicon layer by SLS technique; forming an active layer by etching the crystallized silicon layer through photolithography; and forming source and drain electrodes connecting the active layer electrically.

Specific embodiments will now be described, by way of example, with reference to the accompanying drawings, in which:

Figs. 1A to 1E are schematic drawings of a TFT according to prior art;

Figs. 2A to 2E are schematic drawings of a TFT according to a first embodiment of the present invention;

Figs. 3 to 5 are schematic drawings of a three silicon layer crystallized by SLS technique; and

Figs. 6A to 6E are schematic drawings of a TFT according to a second embodiment of the present invention.

Reference will now be made in detail to the preferred embodiment of the present invention, an example of which is illustrated in the accompanying drawings.

Fig. 2A to Fig. 2E are schematic drawings for explaining a method for fabricating a TFT according to a first embodiment of the present invention. Referring to Fig. 2A, a source electrode 21S and a drain electrode 21D are formed on a insulating substrate 200. An amorphous silicon layer 22 is then deposited on the exposed surface of the substrate comprising the source electrode 21S and the drain electrode 21D. Herein, the amorphous silicon layer 22 has steps and sloping surfaces, since the amorphous silicon layer covers the protruding source and drain electrodes 21S and 21D.

Referring to Fig. 2B, the amorphous silicon layer 22 is crystallized into a polycrystalline silicon layer 23 by using a sequential lateral solidification (SLS) technique. Herein, polycrystalline silicon layer has long columnar silicon grains.

SLS technique uses a phenomenon whereby the grain boundaries in directionally solidified materials tend to form so as to always be approximately perpendicular to the melt interface. The SLS technique enables the

conversion of as-deposited amorphous or polycrystalline silicon films to a directionally solidified microstructure consisting of long, columnar grains (Robert S. Sposilli, M. A. Crowder, and James S. Im, Mat. Res. Soc. Symp. Proc. Vol. 452, 956~957, 1997). Referring to Fig. 3 to Fig. 5, the method for crystallizing the amorphous silicon layer into the polycrystalline silicon layer by SLS technique is described as follows. For convenience of describing such technique, three techniques of the SLS method are taken as examples.

SLS is a technique that forms the silicon layer, by applying laser to an amorphous silicon layer. Here, the displacement of the laser beam is shorter than the length of lateral growth of the crystal. Consequently, silicon particles which are longer than 10 μm are formed on a glass substrate. The foregoing technique is disclosed in "Crystalline Si Films For Integrated Active Matrix Liquid-Crystal Displays," MRS Bulletin, Volume XXI, Number 3, March 1996, pp. 39~48.

Moreover, the location, size, and shape of a crystal particle may be controlled by manipulating the shape of a slit through which a laser beam passes, which enables the formation of silicon particles that are larger than an active area of a TFT. Thus, it is possible to fabricate a TFT of single crystalline silicon manufactured by forming an active area of the TFT as a single crystal particle.

Fig. 3 is schematic drawings for explaining the method for crystallizing the silicon film having large silicon grains according to a first example of the SLS technique. A plurality of the selected regions,

preferably chevron-shaped and having a round apex, of the film are irradiated at an energy density sufficient to induce complete melting. Subsequently, lateral grain growth proceeds from the unmelted regions adjacent to the narrow strip to the fully-melted regions. The grain boundaries in directionally solidified materials tend to form so as to always be approximately perpendicular to the melt interface. Here, the grains formed at the apex of the chevron experience lateral growth not only in the translation direction, but also transverse to it, due to the fact that grain boundaries form roughly perpendicular to the melt interface. Thus, the negative curvature of the molten zone at the apex of the chevron leads to widening of the grain, such that a single crystal silicon grain region is induced.

The film is translated relative to the beam image over a distance less than the single-pulse lateral growth distance, such as approximately one-half of the single-pulse lateral growth distance, and irradiated again. Lateral growth recommences from the edges of the completely molten region, one of which is located within the grains grown during the previous irradiation step. The length of the grains is increased beyond the single-pulse lateral growth distance. Here, the grain formed at the apex of the chevron, a single crystal silicon region, widen. The above-cited process, irradiating and solidifying, can be repeated indefinitely, leading to grains of any desired length. The final structure obtained in this fashion is shown in Fig. 3. The grain formed at the apex of the chevron, a single crystal silicon region, widen dramatically.

Fig. 4 is schematic drawing for explaining the

method for crystallizing the silicon film having large silicon grains according to a second example of the SLS technique. A plurality of the selected narrow regions having a directionally straight shape of the film in a row are irradiated at an energy density sufficient to induce complete melting. Subsequently, lateral grain growth having columnar direction proceeds from the unmelted regions adjacent to the narrow strips to the fully- melted regions. The grain boundaries in directionally solidified materials tend to form so as to always be approximately perpendicular to the melt interface. And the film is translated relative to the beam image over a distance less than the single-pulse lateral growth distance, and irradiated again. Lateral growth recommences from the edges of the completely molten region, one of which is located within the grains grown during the previous irradiation step. The length of the grains is increased beyond the single-pulse lateral growth distance. And, the above cited process, irradiating and solidifying, can be repeated indefinitely, leading to grains of any desired length.

Then, a plurality of the columnar directional selected straight regions of the crystallized silicon film having columnar grains are irradiated. Herein the columnar direction is perpendicular to the row direction. Subsequently, lateral grain growth proceeds in the row direction from the unmelted regions adjacent to the narrow strips to the fully-melted regions, by using one of the first direction columnar grains as seed for grain growth. The grain boundaries in directionally solidified materials tend to form so as to always be approximately perpendicular to the melt interface. And, the above

cited process, irradiating and solidifying, can be repeated indefinitely, leading to grains of any desired length. As the lateral grain growth in row direction proceeds, the seed grain grows more and more. A plurality of the seed grain grows dramatically to form a plurality of the single crystalline region G as the result of the crystallization. Thereby, crystallized silicon film having very large size of the single crystalline regions could be formed on the glass substrate.

Fig. 5 is a schematic drawing for explaining the method for crystallizing the silicon film having large silicon grains according to a third example of the SLS technique. A portion, except a plurality of selected dot regions, is first irradiated at an energy density sufficient to induce complete melting. The amorphous film is translated relative to the laser beam in a first direction over a distance less than one pulse lateral grain growth for second irradiating. While the film is translating, the unmelted dot region of the amorphous silicon is used as seeds and grows into the fully-melted regions. The grain boundaries in directionally solidified materials tend to form so as to always be approximately perpendicular to the melted interface. In addition, portion, except a plurality of selected dot regions, is second irradiated at an energy density sufficient to induce complete melting. Herein the dot region is located in the crystallized silicon region.

The dot region which is not irradiated remains a solid state of the polycrystalline silicon and has a limited number of silicon grains. The amorphous film is translated relative to the laser beam in a second

direction over a distance less than one pulse lateral grain growth for third irradiating. While the amorphous film is being translated, the unmelted dot region of the polycrystalline silicon having three grains is used as seed and grows into the fully-melted regions. A portion, except a plurality of the selected dot regions, is irradiated for a third time at an energy density sufficient to induce complete melting. Herein the dot region is located in the crystallized silicon region. The dot region which is not irradiated remains a solid state of the polycrystalline silicon and has fewer silicon grains than the previous step. Accordingly, as the above process is further carried out, the number of grains in dot region is reduced. Finally, only a single grain remains in the dot region when the appropriate number of above process is carried out.

The size of the single crystalline silicon region is the same as the lateral grain growth. The length of the lateral grain growth depends on the thickness of the film and the temperature of the film. Accordingly, the size of the single crystalline silicon region could be controlled according to the thickness and the temperature of the film. When the distance between the dots is smaller than the length of the lateral grain growth, the polycrystalline silicon film has a plurality of the single crystalline silicon region with grain boundary which is at the interface of the silicon grain and the adjacent silicon grains.

Referring to Fig. 2B, the amorphous silicon layer 22 is crystallized by the SLS technique as described above. A crystallized silicon thin film 23 having a dramatically large first silicon grain 23-1, a second silicon grain

23-2 and a third silicon grain 23-3 are shown in Fig 2B. Herein, the shape and translation distance of the laser beam must be controlled so that the boundaries of the grain to the grain is preferably not located in an active layer of TFT which will be formed.

The laser beam is applied non-vertically to the sloping surface while the laser beam is applied vertically to the flat surface. Although the sloping surface and the flat surface of the amorphous silicon layer are irradiated with laser beam having same laser energy density, the absorbed energy density of the sloping surface may be lower or higher than that of the flat surface. According, it is necessary to use a laser beam having the energy density so as to melt the sloping surface as well as the flat surface of the amorphous silicon layer. For example, when the sloping surface of the amorphous silicon layer could be melted with laser beam having a first energy density or more and the flat surface of the amorphous silicon layer could be melted with laser beam having a second energy density or more, it is necessary to use laser beam having the higher energy density of the two energy densities, the first energy density and the second energy density, so as to melt the sloping surface as well as the flat surface of the amorphous silicon layer.

The necessary laser energy density is in proportion to the angle of the inclination of the amorphous silicon surface. The present embodiment is effectively applied to the case in which the silicon layer having sloping portions with 45 degrees or less of the inclination angle is formed.

Referring to Fig. 2C, the crystallized silicon thin

film is etched by photolithography to form an active layer 24. Since the first silicon grain, the second silicon grain and the third silicon grain are dramatically large, the active layer is formed within one single silicon grain, particularly in the second silicon grain 23-2. Accordingly, a single crystalline silicon TFT could be fabricated on the insulating substrate, such as a glass substrate.

Referring to Fig. 2D, a gate insulating interlayer 25 and a gate electrode 26 are formed on the active layer. Then, a source region 24S and a drain region 24D are formed in the active layer by doping impurities in the exposed portions of the active layer. The channel region 24C is formed between the source region and the drain region.

Referring to Fig. 2E, a passivation layer 27 is deposited on the exposed surface of the substrate and is etched selectively to expose a portion of the drain electrode 21D. And a pixel electrode 28 is formed connecting the exposed portion of the drain electrode on the passivation layer.

Fig. 6A to Fig. 6D are schematic drawings for explaining a method for fabricating a TFT according to a second embodiment of the present invention.

Referring to Fig. 6A, a gate electrode 61 is formed on a insulating substrate 600. And a gate insulating interlayer 62 is deposited on the exposed surface of the substrate comprising the gate electrode. Herein, the gate insulating interlayer 62 has steps and sloping surfaces, since the gate insulating interlayer covers the protruding gate electrode 61.

Referring to Fig. 6B, an amorphous silicon layer is

deposited on the exposed gate insulating interlayer and is crystallized into a polycrystalline silicon layer 63 by an SLS technique described as the above. A crystallized silicon thin film 63 having a dramatically large first silicon grain 63-1, a second silicon grain 63-2 and a third silicon grain 63-3 are shown in Fig 6B. Herein, the shape and translation distance of the laser beam must be controlled so that the boundaries of the grain to the grain are not located in an active layer of TFT which will be formed.

As the above SLS technique proceeds, it is necessary to use a laser beam having the energy density sufficient so as to melt the sloping surface as well as the flat surface of the amorphous silicon layer.

Referring to Fig. 6C, the crystallized silicon thin film is etched by photolithography to form an active layer 63. Since the first silicon grain, the second silicon grain and the third silicon grain are dramatically large, the active layer 63 is formed in one single silicon grain. Accordingly, a single crystalline silicon TFT could be fabricated on the insulating substrate, such as a glass substrate.

Referring to Fig. 6D, a source and a drain electrodes 65S and 65D connect the active layer 63 electrically, thereby fabricating a stagger-type single crystalline silicon TFT on the substrate. Ohmic contact layers 64 could be formed in the interface of the active layer and the source and drain electrodes. And a passivation layer 66 is deposited on the exposed surface of the substrate and is etched selectively to expose a portion of the drain electrode 65D. And a pixel electrode 67 is formed connecting the exposed portion of

the drain electrode on the passivation layer.

According to the embodiments, the polycrystalline silicon layer having large silicon grains could be formed on the substrate by SLS technique. The crystallized silicon layer is etched by photolithography to form the active layer of the TFT. Accordingly, co-planar or stagger-type single crystalline silicon TFT could be formed on the substrate by SLS technique.

The embodiments enable one to fabricate a System On Panel (SOP)-type LCD, in which a pixel part, a driver, a controller and a CPU circuit is fabricated on the same substrate, whereby the fabrication process is simplified and the productivity is increased. Moreover, it is possible to fabricate a portable product of the LCD reduced in weight and size, since the space occupied by the controller and the CPU circuit is reduced.

It will be apparent to those skilled in the art that various modifications and variations can be made in a SOP-type liquid crystal display of the present embodiments without departing from the spirit or scope of the inventions. Thus, it is intended that the present invention will cover the modifications and variations of this invention provided they come within the scope of the appended claims and equivalents.

CLAIMS

1. A method for fabricating a TFT having an active layer, comprising:

crystallizing an amorphous silicon layer having a sloping surface and a flat surface by SLS technique using a laser beam having sufficient energy density to substantially melt the sloping surface and the flat surface of the amorphous silicon layer to form a crystallized silicon layer; and

forming the active layer by selectively etching the crystallized silicon layer.

2. The method according to claim 1, wherein the TFT is a stagger type TFT.

3. The method according to claim 1, wherein the TFT is an inverted stagger type TFT.

4. The method according to any of claims 1 to 3, wherein the energy density of the laser beam required to substantially melt the sloping surface is higher than that of the flat surface and the amorphous silicon layer is irradiated with the energy density required to substantially melt the sloping surface.

5. The method according to any of claims 1 to 4, wherein the energy density of the laser beam required to substantially melt the sloping surface is proportional to the angle of the sloping surface with respect to the flat surface.

6. The method according to any of claims 1 to 5, wherein the sloping surface is about 45 degrees or less with respect to the flat surface.

7. The method according to any of claims 1 to 6, wherein the laser beam requires first energy density to substantially melt the sloping surface and second energy density to substantially melt the flat surface of the amorphous silicon, and wherein the amorphous silicon layer is irradiated with the laser beam having the first energy density.

8. A method for fabricating a TFT, comprising:

forming source and drain electrodes on a substrate;

depositing an amorphous silicon layer on the exposed portion of the substrate having the source and the drain electrodes, the amorphous silicon layer forming at least one sloping surface and one flat surface;

crystallizing the amorphous silicon layer with a laser beam by using SLS technique, the laser beam having sufficient energy density to substantially melt the sloping surface and the flat surface of the amorphous silicon layer, wherein the sloping surface is generated from the amorphous silicon layer covering at least one of the protruding source and the drain electrodes;

forming an active layer by etching the crystallized silicon layer through photolithography;

forming a gate electrode and a gate insulating layer on the active layer; and

forming source and drain regions in the active layer by doping impurities selectively in the exposed portion of the active layer.

9. The method according to claim 8, wherein the laser beam requires first energy density to substantially melt the sloping surface and second energy density to substantially melt the flat surface of the amorphous silicon, and wherein the amorphous silicon layer is irradiated with the laser beam having the first energy density.

10. The method according to claim 8 or 9, wherein the energy density of the laser beam required to substantially melt the sloping surface is proportional to the angle of the sloping surface with respect to the flat surface.

11. The method according to any of claims 8 to 10, wherein the sloping surface is about 45 degrees or less with respect to the flat surface.

12. A method for fabricating a TFT, comprising:

forming a gate electrode on a substrate;

forming a gate insulating layer on the exposed portion of the substrate comprising the gate electrode;

depositing an amorphous silicon layer on the exposed portion of the gate insulating layer, the amorphous silicon layer forming at least one sloping surface and one flat surface;

crystallizing the amorphous silicon layer with a laser beam by using SLS technique, the laser beam having sufficient energy density to substantially melt the sloping surface and the flat surface of the amorphous silicon layer;

forming an active layer by etching the crystallized

silicon layer through photolithography; and

forming source and drain electrodes on the active layer.

13. The method according to claim 12, wherein the sloping surface is generated from the amorphous silicon layer covering the protruding gate electrode.

14. The method according to claim 12 or 13, wherein the laser beam requires first energy density to substantially melt the sloping surface and second energy density to substantially melt the flat surface of the amorphous silicon, and wherein the amorphous silicon layer is irradiated with the laser beam having the first energy density.

15. The method according to any of claims 12 to 14, wherein the energy density of the laser beam required to substantially melt the sloping surface is proportional to the angle of the sloping surface with respect to the flat surface.

16. The method according to any of claims 12 to 15, wherein the sloping surface is about 45 degrees or less with respect to the flat surface.

17. A method of fabricating a TFT as substantially hereinbefore described with reference to and/or substantially as illustrated in any one of or any combination of Figs. 2A to 6E of the accompanying drawings.

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Databases searched:

UK Patent Office collections, including GB, EP, WO & US patent specifications, in:

UK Cl (Ed.Q): H1K(KLHA,KLXW)

Int Cl (Ed.6): H01L 21/20; 21/336

Other: Online: WPI, JAPIO, EPODOC

Documents considered to be relevant:

Category	Identity of document and relevant passage		Relevant to claims
A	US 5 817 548	(SONY)	
A	US 5 432 122	(GOLDSTAR)	

X	Document indicating lack of novelty or inventive step	A	Document indicating technological background and/or state of the art.
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